

CLAIM AMENDMENTS

1 1. (currently amended) A method of exchanging data
2 within a direct memory access ~~[[DMA]]~~ arrangement including a
3 plurality of IP blocks, the method comprising (A, B, C),
4 ~~characterized in that it includes the steps of: [[-]]~~

5 associating with said IP blocks ~~[(A, B, C)]~~ respective
6 DMA modules ~~(IDMA A, IDMA B, IDMA C),~~ each of ~~said DMA modules~~
7 including an input buffer ~~[(11A, 11B, 11C)]~~ and an output buffer
8 ~~[(12A, 12B, 12C)]; [[-]]~~

9 coupling said respective DMA modules ~~[(IDMA A, IDMA B,~~
10 IDMA C)] over a data transfer facility ~~[(BUS)]~~ in a chain
11 arrangement where ~~[[in]]~~ each ~~[[said]]~~ DMA module, other than the
12 last in the chain, has ~~at least one of its~~ respective output
13 buffers ~~[(12A, 12B)]~~ coupled to the input buffer ~~[(11B, 11C)]~~
14 of another of said DMA modules downstream in the chain and each of
15 said DMA modules, other than the first in the chain, has its
16 respective input buffer ~~[(11B, 11C)]~~ coupled to the output buffer
17 ~~[(12A, 12B)]~~ of another of said DMA modules upstream in the
18 chain; ~~[[-]]~~

19 causing each of said DMA modules ~~[(IDMA A, IDMA B, IDMA~~
20 C)] to interact with the respective IP block ~~[(A, B, C)]~~ by
21 writing data from the input buffer ~~[(11A, 11B, 11C)]~~ of the
22 ~~[[I]]~~ DMA module into the respective IP block ~~[(A, B, C)]~~ and
23 reading data from the respective IP block ~~[(A, B, C)]~~ into the
24 output buffer ~~[(12A, 12B, 12C)]~~ of the DMA module; and ~~[[-]]~~

25 operating said input [[(11A, 11B, 11C)]] and output
26 [[(12A, 12B, 12C)]] buffers in such a way that: [[-]]
27 said writing of data from the input buffer [[(11A,
28 11B, 11C)]] of the DMA module into the
29 respective IP block [[(A, B, C)]] is started
30 when [[said]] the respective input buffer
31 [[(11A, 11B, 11C)]] is at least partly filled
32 with data; and [[-]]
33 when said reading of data from the respective IP
34 block [[(A, B, C)]] into the output buffer of
35 the DMA module is completed, the data in the
36 output buffer of the DMA module are transferred
37 to the input buffer [[(11B, 11C)]] of the DMA
38 module downstream in the chain or, in the case
39 of the last DMA module in the chain, are
40 provided as output data.

1 2. (currently amended) The method of claim 1, charac-
2 ~~terized in that it includes~~ further comprising the steps of: [[-]]
3 associating [[to]] with said output buffers [[(12A,
4 12B)]] and input buffers [[(11B, 11C)]] coupled in the chain at
5 least one intermediate block [[(16A, 16B)]] to control data
6 transfer between said coupled buffers; [[-]] and
7 controlling transfer of data between said coupled buffers
8 over said data transfer facility by [[: -]] issuing at least one
9 request of a requesting buffer for a buffer coupled therewith to

10 indicate at least one transfer condition selected out of the group
11 consisting of:

12 data existing to be transferred and enough space
13 existing for receiving said data when
14 transferred; [[-]]

15 issuing at least one corresponding acknowledgment
16 towards said requesting buffer confirming that
17 the said at least one transfer condition is
18 met; and [[-]]

19 transferring data between said requesting buffer and
20 said coupled buffer, whereby said data transfer
21 facility [[(BUS)]] is left free between said at
22 least one request and said at least one
23 acknowledgement.

1 3. (currently amended) The method of either of claims 1
2 or 2, ~~characterized in that it comprises~~ further comprising the
3 steps of: [[-]]

4 including a CPU in said arrangement; [[and -]]

5 using said CPU for transferring data to be processed into
6 the input buffer [[(11A)]] of the first DMA module [[(IDMA A)]] in
7 said chain; and [[-]]

8 using said CPU for collecting said output data from the
9 output buffer [[(12C)]] of the last DMA module [[(IDMA C)]] in said
10 chain.

1 4. (currently amended) The method of claim 3,
2 ~~characterized in that it includes~~ further comprising the step of
3 configuring said DMA modules ~~[[IDMA A, IDMA B, IDMA C]]~~
4 via said CPU.

1 5. (currently amended) Architecture of a direct memory
2 access module ~~[[IDMA]]~~ for exchanging data between a plurality of
3 IP blocks, ~~characterized in that it includes~~ the architecture
4 comprising: ~~[[]]~~

5 a data transfer facility ~~[[BUS]]~~; ~~[[]]~~

6 a plurality of respective DMA modules ~~[[IDMA A, IDMA B,~~
7 IDMA C]] associated with said IP blocks, the DMA modules being
8 coupled over said data transfer facility ~~[[BUS]]~~, each DMA module
9 including: ~~[[]]~~

10 an input buffer ~~[[11]]~~ arranged for writing data
11 into a respective IP block ~~[[A, B, C]]~~ and
12 exchanging data with said data transfer
13 facility ~~[[BUS]]~~, and ~~[[]]~~

14 an output buffer ~~[[12]]~~ arranged for reading data
15 from said respective IP block ~~[[A, B, C]]~~ and
16 exchanging data with said data transfer ~~[[s]]~~
17 facility, ~~(BUS)~~; wherein said DMA modules
18 ~~[[are]]~~ being arranged in a chain so that each
19 of said DMA modules, other than the last in the
20 chain, has ~~at least one of its~~ respective
21 output buffer ~~[[12A, 12B]]~~ coupled to the

22 input buffer [[(11B, 11C)]] of another of said
23 DMA modules downstream in the chain and each of
24 said DMA modules, other than the first in the
25 chain, has its input buffer [[(11B, 11C)]]
26 coupled to the output buffer [[(12A, 12B)]] of
27 another of said DMA modules upstream in the
28 chain.

1 6. (currently amended) The architecture of claim 5 ~~7~~
2 ~~characterized in that wherein~~ at least one of said input [[(11)]]
3 and output [[(12)]] buffers has a fixed data width with respect to
4 said data transfers facility [[(BUS)]] and a selectively variable
5 data width with respect to said respective IP blocks [[(A, B, C)]].

1 7. (currently amended) The architecture of ~~either of~~
2 claim [[s]] 5 or 6, ~~characterized in that it includes~~ further
3 comprising

4 a slave interface module [[(18)]] configured for reading
5 from outside the architecture data relating to at least one
6 parameter selected from the group consisting of: [[-]]

7 how many bits are available for reading in said
8 input buffer [[(11)]], [[-]]

9 how many bits are present in said input buffer
10 [[(11)]], [[-]]

11 how many bits are available for reading in said
12 output buffer [[(12)]], and [[-]]

13 how many bits are present in said output buffer
14 [[(12)]].

1 8. (currently amended) The architecture of ~~any of~~
2 ~~claims claim~~ 5 to 7, ~~characterized in that it includes further~~
3 ~~comprising~~

4 a reprogrammable finite state machine [[(13)]] arranged
5 for driving operation of said architecture by taking data from said
6 input buffer [[(11)]], downloading data into said respective IP
7 block [[(A, B, C)]], receiving data from said respective IP block
8 [[(A, B, C)]], and storing data in said output buffer [[(12)]].

1 9. (currently amended) The architecture of ~~any of~~
2 ~~claims claim~~ 5 to 8, ~~characterized in that to wherein~~ at least one
3 of said input buffers [[(11)]] and output buffers [[(12)]]
4 [[there]] is associated with a respective master block [[(15,16)]]
5 for exchanging data between the associated buffer [[(11,12)]] and
6 said data transfer facility [[(BUS)]], said master block
7 [[(15,16)]] being adapted to be coupled in a data exchange
8 relationship to a buffer in a homologous direct memory access
9 module [[(IDMA)]] in an arrangement wherein said master block
10 [[(15,16)]] and said buffer coupled thereto are configured for:
11 [[-]]

12 issuing at least one request of a requesting buffer for a
13 buffer coupled therewith to indicate at least one transfer
14 condition selected out of the group consisting of [[:]]

15 data existing to be transferred and enough space existing
16 for receiving said data when transferred; [[-]]
17 issuing at least one corresponding acknowledgement
18 towards said requesting buffer confirming that the said at least
19 one transfer condition is met; and [[-]]
20 transferring data between said requesting buffer and said
21 coupled buffer, whereby said data transfer facility [[(BUS)]] is
22 left free between said at least one request and said at least one
23 acknowledgement.

10. (canceled)